GENERAL SPECIFICATION APPROVAL FOR
TDK MULTILAYER CERAMIC CAPACITORS

CUSTOMER		DWG.NO.
TDK ITEM C1005 TO C5750 TYPE		DATE ISSUED
DRAWN BY	CHECKED BY	APPROVED BY

Customer to Complete

☐ Approved	Office/Division:	Date:
☐ Conditional Approval	Name (Please print):	
☐ Disapproved	Title:	

If you approve, please describe your requests or comments regarding the change. If you reject, please explain your decision by reflecting your requirements for approval:

X	X	X
CUSTOMER SIGNATURE	TITLE	DATE (mm/dd/yy)

TDK®

TDK®

Multilayer Ceramic Capacitors

General Specification for C1005 ~ C5750

April 2003

Contents **Page**

1.0 Introduction

1.1 Scope

This specification is applicable to TDK chip type multilayer ceramic capacitors. When questionable matters arise regarding product specifications, this specification shall be applicable with priority and the matters shall be settled with written documents between the Design Groups of both companies. Production locations defined in this specification shall be TDK Corporation Japan, TDK Taiwan, TDK Xiamen (CHINA), TDK Suzhou (CHINA), Korea TDK, TDK Components USA, TDK Thailand, TDK Malaysia and TDK Hungary.

EXPLANATORY NOTE:
This specification warrants the quality of the TDK ceramic chip capacitor. The chips should be evaluated or confirmed by mounting the component on your board. If the use of the capacitor extends beyond the bounds of this specification, we can not guarantee its performance. This specification is subject to change without notice. Please contact your local TDK Sales Representative for all current documentation.

1.2 Storage

TDK multilayer ceramic chip capacitors will not lose their electrical characteristics in ambient conditions; however, solderability and taping properties may change during extended storage. Therefore, the following precautionary measures are recommended:

- Storage Environment:

The packaging of chip capacitors is designed to have a long shelf life, but in order to minimize the aging of the packaging materials, storage conditions should be less than 40°C and under 70% relative humidity. Use TDK multilayer ceramic chip capacitors within six months of receiving.

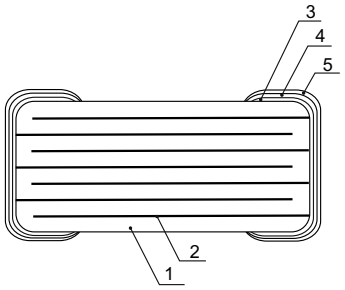
- Atmosphere:

Chlorine gas or sulfuric acid in the air may adversely affect the solderability of the termination, therefore, avoid exposure to this environment.

- Rapid temperature changes:

When removing TDK multilayer ceramic chip capacitors from their storage place, avoid any differences in temperature that would cause moisture condensation.

1.3 MLCC Inner Structure



No.	Name	Material			
		Class I		Class II, III	
		Pd	TME	Pd	TME
1	Dielectric	TiO_2	$CaZrO_3$	$BaTiO_3$	
2	Electrode	Pd	Ni	Pd	Ni
3	Termination	Ag or Ag/Pd	Cu	Ag or Ag/Pd	Cu
4		Ni			
5		100% Sn			

Figure 1.3: MLCC Inner Structure

2.0 Number Description - the TDK item number and inspection number are described herein.

2.1 Item Number Description

(Example) **C3216** (1) **X7R** (2) **1C** (3) **335** (4) **K** (5) **T** (6) **XXXX** (7)

(1) Case Size

See Table 2.1 for details.

(2) Temperature Characteristics

	T.C.	Temp. Range	Temp. Coefficient (ppm/°C)
Class I	C0G	-55 to 125 °C	0 ± 30
	T.C.	**Temp. Range**	**Capacitance Change (%)***
Class II, III	X7R	-55 to 125 °C	± 15
	X5R	-55 to 85 °C	
	Y5V	-30 to 85 °C	+22/-82

* No Voltage Applied

(3) Rated Voltage

Numeric Prefix	Rated Voltage Alpha Code					
	J	A	D	C	E	H
0	6.3	-	-	-	-	-
1	-	10	-	16	25	50
2	630	100	-	-	250	-

Unit : Volts

(4) Rated Capacitance

Stated in three digits and in units of picofarads (pF). The first and second digits identify the first and second significant figures of the capacitance, the third digit identifies the multiplier. R is designated for a decimal point.

Examples

335 -- 3,300,000 pF (3.3μ F)
3R5 -- 3.5 pF
010 -- 1 pF

(5) Capacitance Tolerance

Symbol	Tolerance	Capacitance
B	± 0.1 pF	10 pF and under
C	± 0.25 pF	
D	± 0.5 pF	
F	± 1 pF	
F	± 1%	over 10pF
G	± 2%	
J	± 5 %	
K	± 10%	
M	± 20%	
Z	+80%, - 20%	

(6) Packaging

T -- Taping
B -- Bulk
C -- Cassette

(7) TDK's Internal Codes

TDK's internal codes are manufacturing specific and subject to change without notice.

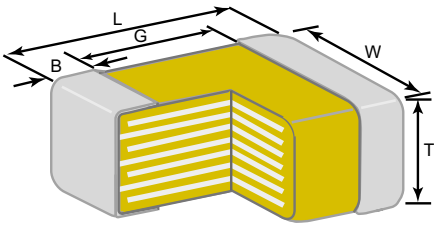
Type TDK (EIA style)	Dimensions[1] (Unit: mm) L	W	T	B	G	Illustration
C1005 (CC0402)	1.0 ± 0.05	0.5 ± 0.05	0.50 ± 0.05	0.10 min.	0.30 min.	
C1608 (CC0603)	1.60 ± [0.07] 0.10	0.80 ± [0.07] 0.10	0.80 ± [0.07] 0.10	0.20 min.	0.30 min.	
C2012 (CC0805)	2.00 ± [0.10] 0.20	1.25 ± [0.10] 0.20	0.60 ± [0.10] 0.15	0.20 min.	0.50 min.	
			0.85 ± 0.15			
			1.25 ± 0.20			
C3216 (CC1206)	3.20 ± [0.10] 0.20	1.60 ± [0.10] 0.20	0.60 ± [0.10] 0.15	0.20 min.	1.00 min.	
			0.85 ± 0.15			
			1.15 ± 0.15			
	3.20 +0.30 -0.10	1.60 +0.30 -0.10	1.30 ± 0.20			
			1.60 +0.30 -0.10			
C3225 (CC1210)	3.20 ± 0.40	2.50 ± 0.30	2.00 ± 0.20	0.20 min.	—	
			2.50 ± 0.30			
C4532 (CC1812)	4.50 ± 0.40	3.20 ± 0.40	1.60 ± 0.20	0.20 min.	—	
			2.30 ± 0.20			
C5750 (CC2220)	5.70 ± 0.40	5.00 ± 0.40	1.60 ± 0.20	0.20 min.	—	
			2.30 ± 0.20			

Table 2.1: Capacitor Dimensions

[1] Tolerance is for tape and reels packaging styles; dimensions inside of [ ] are applied to bulk case.

2.2 Inspection Number

All TDK capacitors will be labeled with an inspection number. The inspection number is assigned only after all QA requirements are confirmed. This number also provides full traceability of all processing details and should be included with any inquiry back to the factory.

Example: M 9 A - XX - XXX
(a) (b) (c) (d) (e)

a) Line code
b) Last digit of the year
c) Month (ex. A for January, B for February, and so on. (Skip "I"))
d) Inspection Date of the month.
e) Serial No. of the day

3.0 Rated Capacitance and Tolerances, Operating Temperature, and Dimensions

3.1 Standard combination of rated capacitances and tolerances

Table 3.1: Rated Capacitances and Tolerances

Class	Temperature Characteristics	Capacitance Tolerance		Rated capacitance
1	C0G	10pF and under	C (± 0.25pF)	1, 1.5, 2, 2.2, 3, 3.3, 4, 4.7, 5
			D (± 0.5pF)	6, 6.8, 7, 8, 9, 10
			F (± 1pF)	6, 7, 8, 9, 10
		over 10pF	J (± 5%)	E - 12 series
			K (± 10%)	
2	X5R, X7R	K (± 10%), M (± 20%)		E - 6 series
3	Y5V	Z (+80%, -20%)		E - 3 series

3.2 Capacitance Step in E series

Table 3.2: Capacitance Step

E series	Capacitance Step											
E - 3	1				2.2				4.7			
E - 6	1		1.5		2.2		3.3		4.7		6.8	
E - 12	1	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2

3.3 Operating Temperature Range

Table 3.3: Operating Temperature Range

T.C.	Min.	Max.	Reference Temperature	Cap Change
C0G	- 55°C	125 °C	25 °C	±30 ppm/°C
X7R	- 55 °C	125 °C	25 °C	±15 %
X5R	- 55 °C	85 °C	25 °C	±15 %
Y5V	- 30 °C	85 °C	25 °C	+22/-82 %

3.4 Dimensions

See Table 2.1: Capacitor Dimensions

4.0 Performance and Test Boards

4.1 Performance

Table 4.1: Performance

<table>
<tr><th>No.</th><th colspan="2">Item</th><th colspan="2">Performance</th><th>Test or inspection method</th></tr>
<tr><td>1</td><td colspan="2">External Appearance</td><td colspan="2">No defects which may affect performance.</td><td>Inspect under 3x magnification.</td></tr>
<tr><td>2</td><td colspan="2">Insulation Resistance</td><td colspan="2">10,000 MΩ or 500MΩ / μF min. (10,000 MΩ or 100MΩ / μF for capacitors rated 16, 10 and 6.3V DC) whichever smaller.</td><td>Apply rated voltage for 60 s.
(For 630V rated voltage, use 500V.)</td></tr>
<tr><td>3</td><td colspan="2">Dielectric Withstanding (DWV)</td><td colspan="2">Withstand test voltage without insulation breakdown or other damage.</td><td>Class 1: 3xRV
Class 2, 3: 2.5xRV
(For 250 & 630V, use 1.5xRV)
(DC voltage shall be applied for 1 ~ 5 s. Charge / discharge current shall not exceed 50mA.)</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">Capacitance</td><td>Class 1</td><td colspan="2">Within the specified tolerance.</td><td><table><tr><th>Capacitance</th><th>Frequency</th><th>Voltage</th></tr><tr><td>1,000 pF and under</td><td>1MHz ± 10%</td><td rowspan="2">1.0 ± 0.2 V r.m.s.</td></tr><tr><td>Over 1,000 pF</td><td>1kHz ± 10%</td></tr></table></td></tr>
<tr><td>Class 2, 3</td><td colspan="2">Within the specified tolerance at 1000 hrs age (per IEC-384-9).</td><td><table><tr><th>Capacitance</th><th>Frequency</th><th>Voltage</th></tr><tr><td>C* ≤ 10μF</td><td>1kHz ± 10%</td><td>1.0 ± 0.2 V r.m.s.</td></tr><tr><td>C* > 10μF</td><td>120Hz ± 10%</td><td>0.5 ± 0.2 V r.m.s.</td></tr></table></td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">Q
(Class 1)</td><td colspan="2">330pF < C* ≥ 30pF</td><td>Q ≥ 1000</td><td rowspan="2"><table><tr><th>Capacitance</th><th>Frequency</th><th>Voltage</th></tr><tr><td>1,000 pF and under</td><td>1MHz ± 10%</td><td rowspan="2">1.0 ± 0.2 V r.m.s.</td></tr><tr><td>Over 1,000 pF</td><td>1kHz ± 10%</td></tr></table></td></tr>
<tr><td colspan="2">C* < 30pF</td><td>Q ≥ 400+(20 X C*)</td></tr>
<tr><td>6</td><td>Dissipation Factor**
(Class 2, 3)</td><td colspan="2"><table><tr><th>T.C.</th><th>Rated Voltage</th><th>D.F.</th></tr><tr><td rowspan="2">X7R</td><td>≥ 25V DC</td><td>0.030 max.</td></tr><tr><td>16V DC</td><td>0.050 max.</td></tr><tr><td>X5R</td><td>10V DC and lower</td><td>0.050 max.</td></tr><tr><td rowspan="5">Y5V</td><td>50V DC</td><td>0.050 max.</td></tr><tr><td>25V DC</td><td>0.075 max.</td></tr><tr><td>16V DC</td><td>0.100 max.</td></tr><tr><td>Below 16V DC</td><td>0.125 max.</td></tr></table></td><td colspan="2"><table><tr><th>Capacitance</th><th>Frequency</th><th>Voltage</th></tr><tr><td>C* ≤ 10μF</td><td>1kHz ± 10%</td><td>1.0 ± 0.2 V r.m.s.</td></tr><tr><td>C* > 10μF</td><td>120Hz ± 10%</td><td>0.5 ± 0.2 V r.m.s.</td></tr></table></td></tr>
</table>

* C denotes rated capacitance.
** Unless otherwise stated.

Table 4.1: Performance (continued)

<table>
<tr><th>No.</th><th>Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td>7</td><td>Temperature Characteristic (Class 1)</td><td>Temperature Coefficient (ppm/°C)
C0G: 0 ± 30
Capacitance drift
Within ± 0.2% or ± 0.05pF, Whichever is larger.</td><td>Temperature Coefficient shall be calculated based on capacitance values referenced at 25°C.

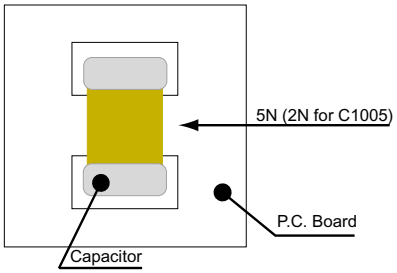
Temperature measured below 20°C shall be at -10°C and -25°C.</td></tr>
<tr><td>8</td><td>Temperature Characteristic (Class 2, 3)</td><td>Capacitance Change (%)*
<table><tr><td>X5R</td><td rowspan="2">± 15</td></tr><tr><td>X7R</td></tr><tr><td>Y5V</td><td>+22/-82</td></tr></table>* No Voltage Applied</td><td>Capacitance shall be measured in the sequence listed in the following table after thermal equilibrium is obtained for each step. See table 3.3 for appropriate temperatures. % Cap change to be calculated using ref. temp. from step 3.
<table><tr><th>Step</th><th>Temperature (°C)</th></tr><tr><td>1</td><td>Reference Temp. ± 2°C</td></tr><tr><td>2</td><td>Min. Temp. ± 2°C</td></tr><tr><td>3</td><td>Reference Temp. ± 2°C</td></tr><tr><td>4</td><td>Max. Temp. ± 2°C</td></tr></table></td></tr>
<tr><td>9</td><td>Terminal Strength</td><td>No sign of termination coming off, breakage of ceramic, or other abnormal signs.</td><td>Glue and wave solder (reflow solder for C1005) the capacitor on a P.C. Board (figure 4.2.2) and apply a pushing force of 5N or (2N for C1005) for 10 ±1s.
 
</td></tr>
</table>

Table 4.1: Performance (continued)

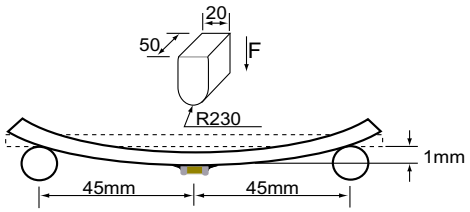
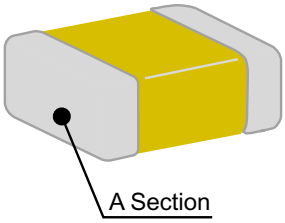
No.	Item	Performance	Test or inspection method
10	Bending	No mechanical damage.	Glue and wave solder (reflow solder for C1005) the capacitor onto a P.C. Board (figure 4.2.1) and bend for 1mm.  (Unit : mm)
11	Solderability	New solder to cover over 75% of termination. 25% may have pinholes or rough spots but not concentrated in one spot. Ceramic surface of A sections shall not be exposed due to melting or shifting of termination material. 	Completely soak both terminations in solder at 235 ± 5°C for 2 ± 0.5s. Apply flux {Isopropyl alcohol (JIS K 8839) and Rosin (JIS K 5902), 25% solid solution} Dip in solder {H63A (JIS Z 3282)}

Table 4.1: Performance (continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td rowspan="6">12</td><td rowspan="6">Resistance to solder heat</td><td>External appearance</td><td>No cracks are allowed and terminations be covered at least 60% with new solder.</td><td rowspan="6">Completely soak both terminations in solder at 260 ± 5°C for 5 ± 1s.

Preheating condition
Temp: 150 ± 10°C
Time: 1 ~ 2 min.

Apply flux
{Isopropyl alcohol (JIS K 8839) and Rosin (JIS K 5902)
25% solid solution}.

Dip in solder
{H63A (JIS Z 3282)}

Leave the capacitors in ambient conditions for the following time before measurement.
Class 1: 24 ± 2hr.
Class 2, 3: 48 ± 4hr.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Change from initial measurement.</th></tr><tr><td rowspan="1">Class 1</td><td>C0G</td><td>± 2.5% or ± 0.25pF max. whichever is larger</td></tr><tr><td rowspan="3">Class 2, 3</td><td>X5R</td><td>± 7.5%</td></tr><tr><td>X7R</td><td>± 7.5%</td></tr><tr><td>Y5V</td><td>± 20 %</td></tr></table></td></tr>
<tr><td>Q (Class 1)</td><td>Meet the initial spec.</td></tr>
<tr><td>DF (Class 2, 3)</td><td>Meet the initial spec.</td></tr>
<tr><td>Insulation resistance</td><td>Meet the initial spec.</td></tr>
<tr><td>DWV</td><td>No insulation breakdown or other damage.</td></tr>
<tr><td rowspan="5">13</td><td rowspan="5">Vibration</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="5">Solder the capacitors on a P.C. Board (figure 4.2.2) before testing.

Apply a waveform with amplitude of 1.5 mm P-P with frequencies sweep from 10Hz to 55Hz and back to 10Hz in about 1 min. Repeat this for 2 hrs each in 3 mutually perpendicular directions.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Change from initial measurement</th></tr><tr><td rowspan="1">Class 1</td><td>C0G</td><td>± 2.5% or ± 0.25pF max. whichever is larger</td></tr><tr><td rowspan="3">Class 2, 3</td><td>X5R</td><td>± 7.5%</td></tr><tr><td>X7R</td><td>± 7.5%</td></tr><tr><td>Y5V</td><td>± 20 %</td></tr></table></td></tr>
<tr><td>Q (Class 1)</td><td>Meet the initial spec.</td></tr>
<tr><td>DF (Class 2, 3)</td><td>Meet the initial spec.</td></tr>
</table>

*C denotes rated capacitance

Table 4.1: Performance (continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td rowspan="6">14</td><td rowspan="6">Temperature cycle</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="6">Solder the capacitors on a P.C. Board (figure 4.2.2) before testing.

Expose the capacitors to the sequence outlined below.(Steps 1-4) See table 3.3 for temp. Repeat steps 1-4 for 5 times consecutively.

<table><tr><th>Step</th><th>Temperature (°C)</th><th>Time (min.)</th></tr><tr><td>1</td><td>Min. Temp. ± 3°C</td><td>30 ± 3</td></tr><tr><td>2</td><td>Reference Temp. ± 2°C</td><td>2 ~ 5</td></tr><tr><td>3</td><td>Max. Temp. ± 2°C</td><td>30 ± 2</td></tr><tr><td>4</td><td>Reference Temp. ± 2°C</td><td>2 ~ 5</td></tr></table>
Leave the capacitors in ambient conditions for the following time before measurement.
Class 1: 24 ± 2hr.
Class 2, 3: 48 ± 4hr.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>% Cap change</th></tr><tr><td rowspan="1">Class 1</td><td>C0G</td><td>± 2.5% or ± 0.25pF max. whichever is larger</td></tr><tr><td rowspan="3">Class 2, 3</td><td>X5R</td><td>± 7.5%</td></tr><tr><td>X7R</td><td>± 7.5%</td></tr><tr><td>Y5V</td><td>± 20 %</td></tr></table></td></tr>
<tr><td>Q (Class 1)</td><td>Meet the initial spec.</td></tr>
<tr><td>DF (Class 2, 3)</td><td>Meet the initial spec.</td></tr>
<tr><td>Insulation resistance</td><td>Meet the initial spec.</td></tr>
<tr><td>DWV</td><td>No insulation breakdown or other damage.</td></tr>
<tr><td rowspan="6">15</td><td rowspan="6">Moisture Resistance (Steady State)</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="6">Solder the capacitors on a P.C. Board (figure 4.2.2) before testing.

Leave at temperature 40 ± 2°C, 90 to 95% relative humidity for 500 +24, -0 hr.

Leave the capacitors in ambient conditions for the following time before measurement.
Class 1: 24 ± 2hr.
Class 2, 3: 48 ± 4hr.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>% Cap change</th></tr><tr><td rowspan="1">Class 1</td><td>C0G</td><td>± 5% or ± 0.5pF max. whichever is larger</td></tr><tr><td rowspan="3">Class 2, 3</td><td>X5R</td><td>± 10%</td></tr><tr><td>X7R</td><td>± 12.5%</td></tr><tr><td>Y5V</td><td>± 30 %</td></tr></table></td></tr>
<tr><td rowspan="3">Q (Class 1)</td><td>C* ≥ 30pF</td><td>Q ≥ 350</td></tr>
<tr><td>30pF>C*≥10pF</td><td>Q ≥ 275+(5/2 X C*)</td></tr>
<tr><td>C* < 10pF</td><td>Q ≥ 200+(10 X C*)</td></tr>
<tr><td>DF (Class 2, 3)</td><td colspan="2">Characteristics
X5R: 200% of Initial spec max.
X7R: 200% of Initial spec max.
Y5V: 150% of Initial spec max.</td></tr>
<tr><td>Insulation resistance</td><td colspan="2">1,000 MΩ or 50 MΩ - μF min. (1,000 MΩ or 10 MΩ - μF for capacitors rated 16, 10 and 6.3V DC.) whichever is smaller.</td></tr>
</table>

*C denotes rated capacitance

Table 4.1: Performance (continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td rowspan="6">16</td><td rowspan="6">Biased Humidity</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="6">Solder the capacitors on a P.C. Board (figure 4.2.2) before testing.

Apply the rated voltage at 85 ± 2°C and 85% relative humidity for 1000 + 48, -0 hr.

Change / discharge current shall not exceed 50mA.

Leave the capacitors in ambient conditions for the following time before measurement.
Class 1: 24 ± 2hr.
Class 2, 3: 48 ± 4hr.

Voltage conditioning: (Class 2, 3 only)
Voltage treat the capacitor under testing temperature and voltage for 1 hour.
Leave the capacitors in ambient condition for 48 ± 4 hrs before Measurement. Use this measurement for the initial value.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Cap change</th></tr><tr><td>Class 1</td><td>C0G</td><td>± 7.5% or ± 0.75pF max. whichever is larger</td></tr><tr><td rowspan="3">Class 2, 3</td><td>X5R</td><td>± 10%</td></tr><tr><td>X7R</td><td>± 12.5%</td></tr><tr><td>Y5V</td><td>± 30 %</td></tr></table></td></tr>
<tr><td rowspan="2">Q (Class 1)</td><td>30pF ≥ C*</td><td>Q ≥ 200</td></tr>
<tr><td>C* < 30pF</td><td>Q ≥ 100+(10/3 X C*)</td></tr>
<tr><td>DF (Class 2, 3)</td><td colspan="2">Characteristics
X5R: 200% of Initial spec max.
X7R: 200% of Initial spec max.
Y5V: 150% of Initial spec max.</td></tr>
<tr><td>Insulation resistance</td><td colspan="2">500 MΩ or 25 MΩ - μF min. (500 MΩ or 5 MΩ - μF for capacitors rated 16, 10 and 6.3V DC.) whichever is smaller.</td></tr>
</table>

*C denotes rated capacitance

Table 4.1: Performance (continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td rowspan="5">17</td><td rowspan="5">Life</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="5">Solder the capacitors on a P.C. Board (figure 4.2.2) before testing.

Voltage conditioning: (Class 2, 3 only)
Voltage treated the capacitor under test temperature and voltage for 1 hr.

Leave the capacitors in ambient condition for 48 ± 4 hr. before measurement.

Use this measurement for initial value.

Apply maximum operating temp ± 2°C for 1000 + 48, -0 hr.
Rated voltage ≤100V: 2xRV
Rated voltage = 250V: 1.5xRV
Rated voltage = 630V: 1.2xRV

Change / discharge current shall not exceed 50mA.

Leave the capacitors in ambient condition for the following time before measurement.
Class 1: 24 ± 2hr.
Class 2, 3: 48 ± 4hr.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Cap change</th></tr><tr><td>Class 1</td><td>C0G</td><td>± 3% or ± 0.3pF max. whichever is larger</td></tr><tr><td rowspan="3">Class 2, 3</td><td>X5R</td><td>± 12.5%</td></tr><tr><td>X7R</td><td>± 15%</td></tr><tr><td>Y5V</td><td>± 30 %</td></tr></table></td></tr>
<tr><td>Q (Class 1)</td><td><table><tr><td>C* ≥ 30pF</td><td>Q ≥ 350</td></tr><tr><td>30pF>C*≥10pF</td><td>Q ≥ 275+(5/2 X C*)</td></tr><tr><td>C < 10pF</td><td>Q ≥ 200+(10 X C*)</td></tr></table></td></tr>
<tr><td>DF (Class 2, 3)</td><td>Characteristics
X5R: 200% of Initial spec max.
X7R: 200% of Initial spec max.
Y5V: 150% of Initial spec max.</td></tr>
<tr><td>Insulation resistance</td><td>1,000 MΩ or 50 MΩ - μF min. (1,000 MΩ or 10 MΩ - μF for capacitors rated 16, 10 and 6.3V DC.) whichever smaller.</td></tr>
</table>

*C denotes rated capacitance

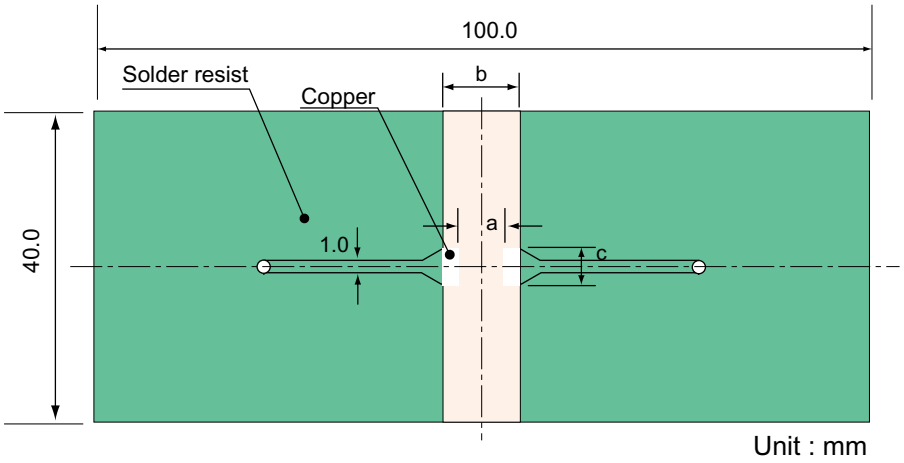
Note: As for the initial measurement of capacitors (Class 2, 3) on number 8, 12, 13,14, and 15, leave capacitors at 150 +0, -10°C for 1 hr. and measure the value after leaving capacitors for 48 ± 4 hr. in ambient condition.

4.2 Test Boards

All the test boards are using the following conditions:

1. Board Material : Glass Epoxy (As per JIS C6484 GE4)
2. Board Thickness : 0.8mm (Board I), 1.6 mm (Board II)
3. Trace Material : Copper with tin overcoat
4. Trace Thickness : Copper (0.035 mm), Tin adequately covered.

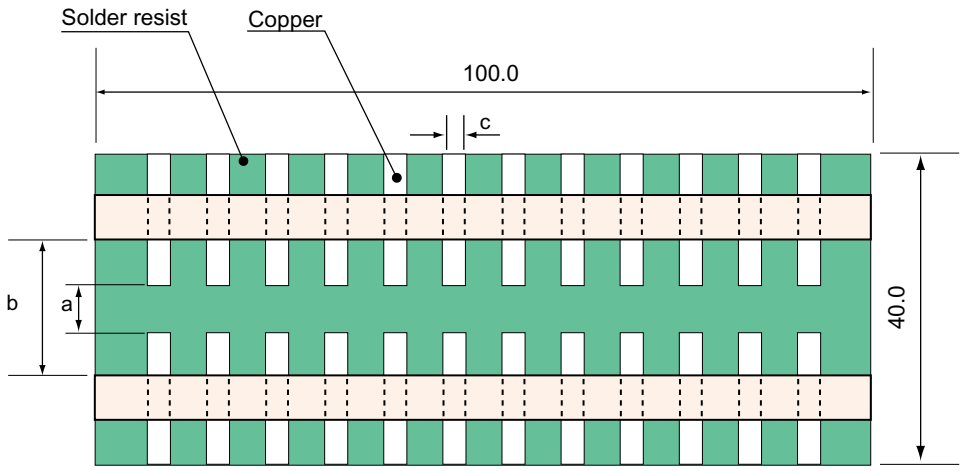
4.2.1. Board I



Type	Dimensions (Unit: mm)		
TDK (EIA Style)	a	b	c
C1005 (CC0402)	0.40	1.50	0.50
C1608 (CC0603)	1.00	3.00	1.20
C2012 (CC0805)	1.20	4.00	1.65
C3216 (CC1206)	2.20	5.00	2.00
C3225 (CC1210)	2.20	5.00	2.90
C4532 (CC1812)	3.50	7.00	3.70
C5750 (CC2220)	4.50	8.00	5.60

Figure 4.2.1: Board I

4.2.2 Board II

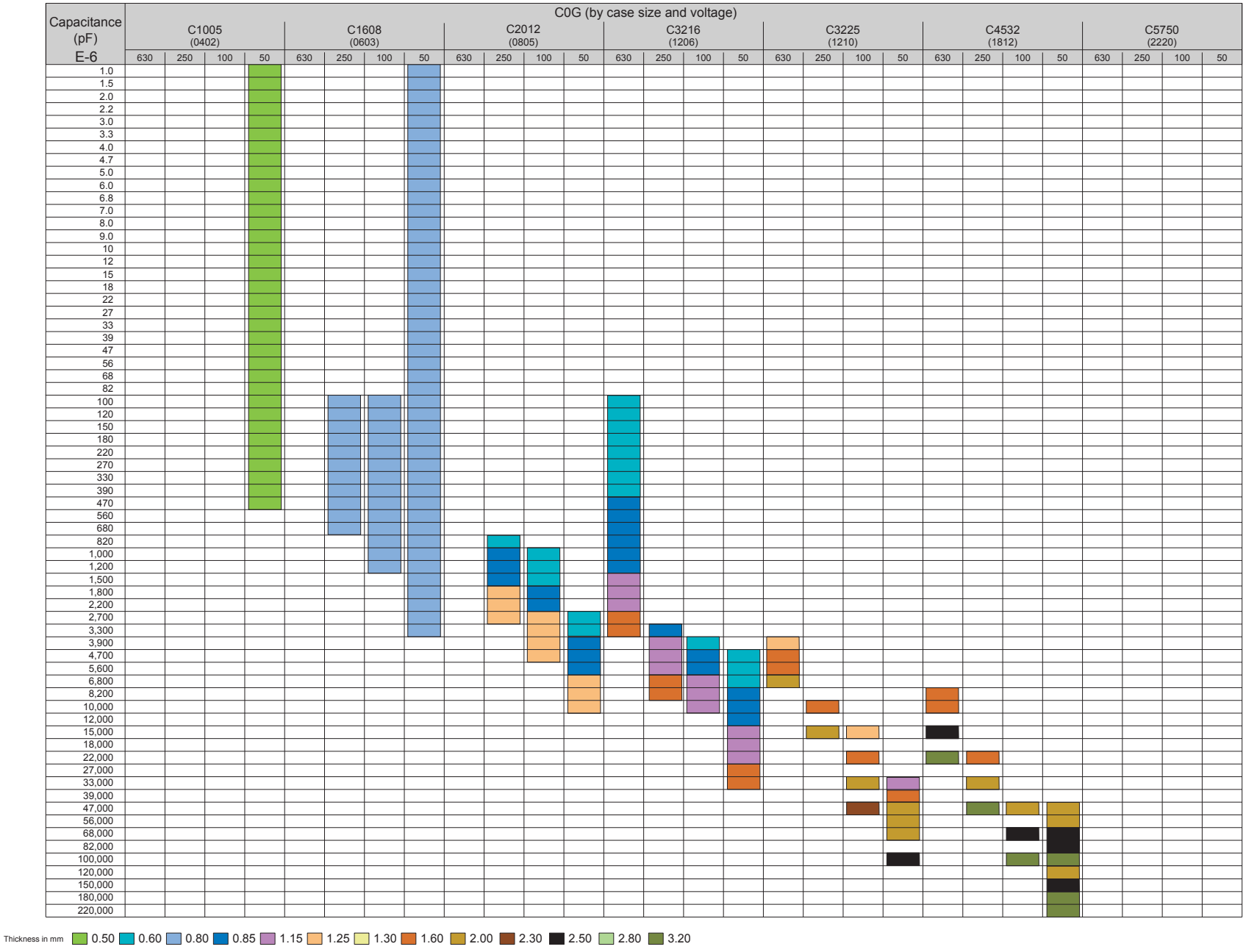


Unit : mm

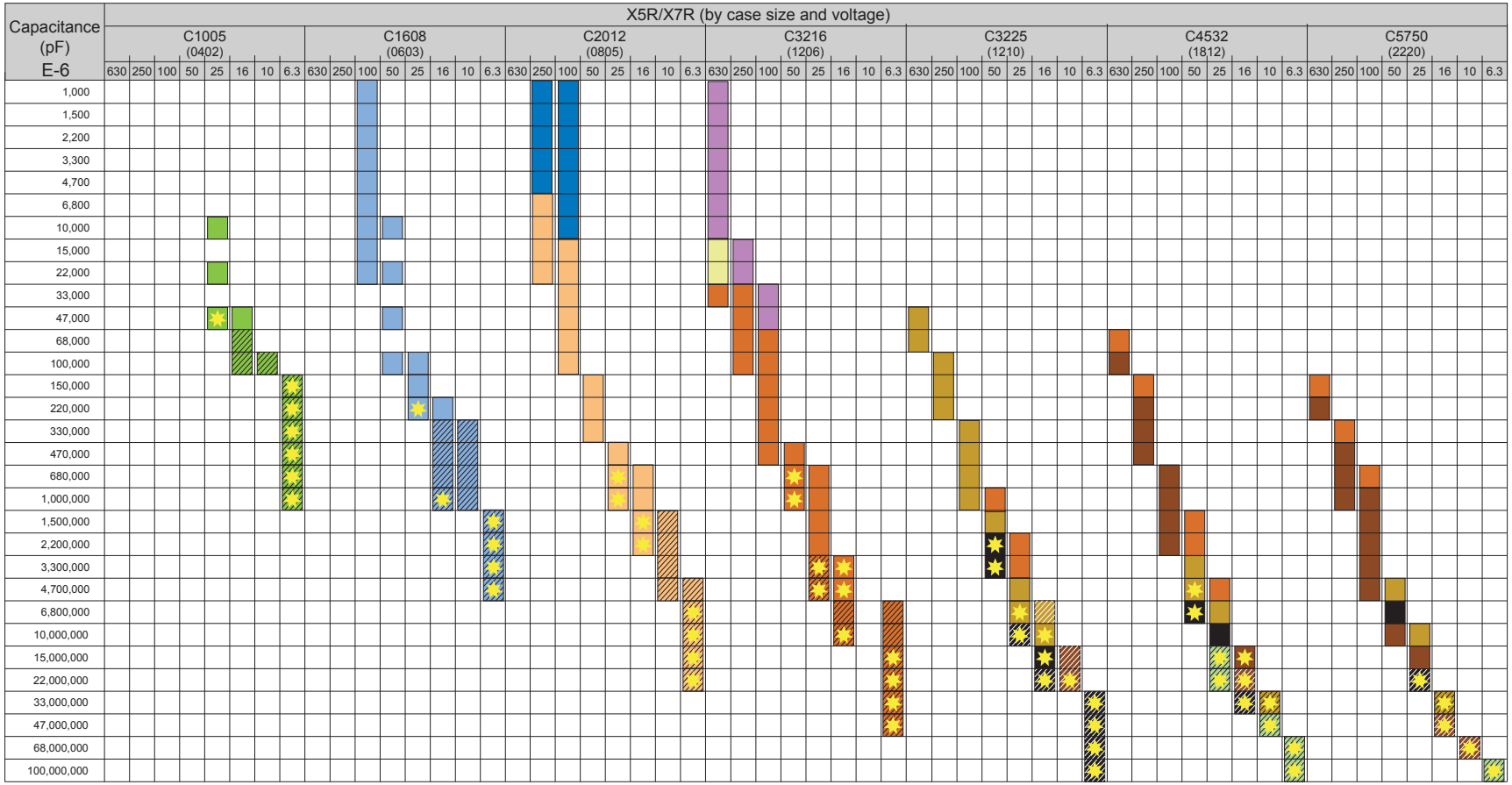
Type	Dimensions (Unit: mm)		
TDK (EIA Style)	a	b	c
C1005 (CC0402)	0.40	1.50	0.50
C1608 (CC0603)	1.00	3.00	1.20
C2012 (CC0805)	1.20	4.00	1.65
C3216 (CC1206)	2.20	5.00	2.00
C3225 (CC1210)	2.20	5.00	2.90
C4532 (CC1812)	3.50	7.00	3.70
C5750 (CC2220)	4.50	8.00	5.60

Figure 4.2.2: Board II

5.0 Available Capacitor Range



5.0 Available Capacitor Range



Thickness in mm 0.50 0.60 0.80 0.85 1.15 1.25 1.30 1.60 2.00 2.30 2.50 2.80 3.20 X5R Contact TDK for Spec

5.0 Available Capacitor Range

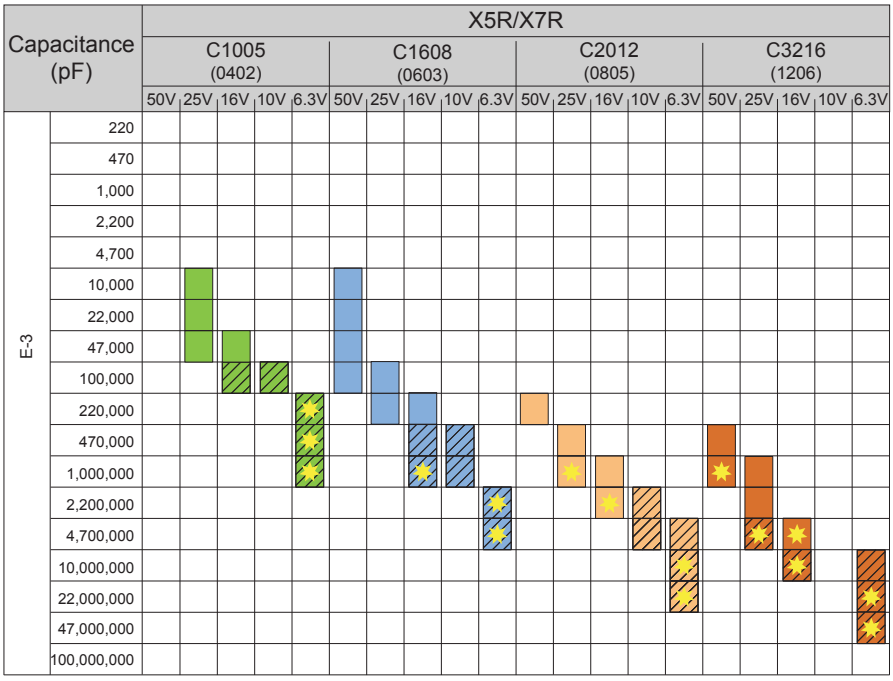
Capacitance (F) E-3	Y5V (by case size and voltage)																															
	C1005 (0402)					C1608 (0603)					C2012 (0805)					C3216 (1206)					C3225 (1210)					C4532 (1812)					C5750 (2220)				
	50	25	16	10	6.3	50	25	16	10	6.3	50	25	16	10	6.3	50	25	16	10	6.3	50	25	16	10	6.3	50	25	16	10	6.3	50	25	16	10	6.3
.01																																			
.022																																			
.047																																			
.1																																			
.22																																			
.47																																			
1																																			
2.2																																			
4.7																																			
10																																			
22																																			
47																																			
100																																			

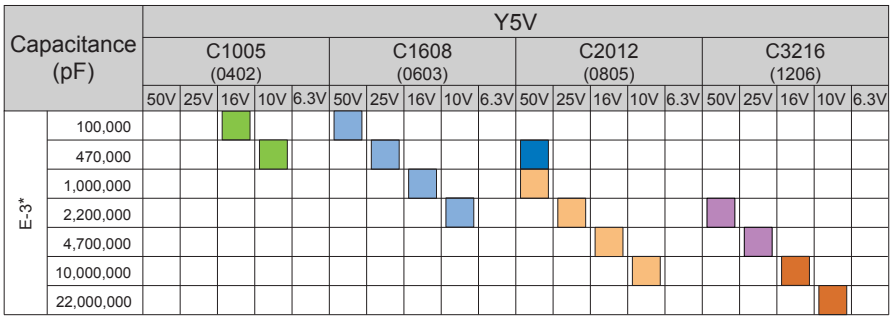
Thickness in mm 0.50 0.60 0.80 0.85 1.15 1.25 1.30 1.60 2.00 2.30 2.50 2.80 3.20

5.1 TDK Standard Capacitors (for 1005-3216 only)

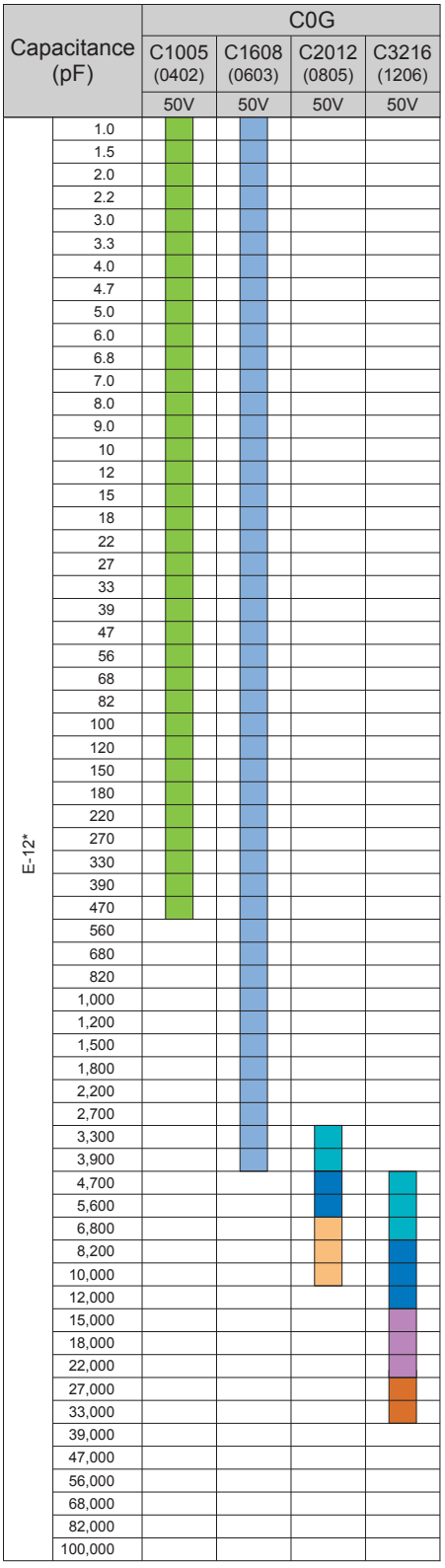
Definition of TDK's "Standard Items"					
Item	C0G		X5R/X7R		Y5V
Capacitance	E-12		E-3		E-3
Tolerance	± 0.25 pF	5 pF	± 10 %	4,700,000 pF	+80%, -20%
	± 0.50 pF	5 pF < and 10 pF			
	± 5 %	> 10 pF	± 20 %	> 4,700,000 pF	
Rated Voltage	Higher rated voltage can be substituted for lower rated voltage.				
Case Size	Highest capacitance in smallest body. (Downsize: C3216,C2012 → C1608,C1005)				
Packaging	Tape & Reel : 10,000 pc.*; 13" reel; EIA 481 leader; plastic carrier tape if t 1.15mm, otherwise paper carrier tape. *Note: 8,000 pc. per 13" reel for 3216 1.6 thickness parts.				

Advantages
- Simplified inventory control
- Improved yield and productivity
- Better delivery
- Better pricing





* 470,000pF



* E-12 series is applied to capacitance values >10 pF

Thickness in mm 0.50 0.60 0.80 0.85 1.15 1.25 1.30 1.60 2.00 2.30 2.50 2.80 3.20 X5R Contact TDK for Spec

5.1 List of Standard Items (for 1005-3216 only)

Case Size	TC	Voltage	Cap (pF)	TDK Item Number
1005	C0G	50	1	C1005C0G1H010CT
1005	C0G	50	1.5	C1005C0G1H1R5CT
1005	C0G	50	2	C1005C0G1H020CT
1005	C0G	50	2.2	C1005C0G1H2R2CT
1005	C0G	50	3	C1005C0G1H030CT
1005	C0G	50	3.3	C1005C0G1H3R3CT
1005	C0G	50	4	C1005C0G1H040CT
1005	C0G	50	4.7	C1005C0G1H4R7CT
1005	C0G	50	5	C1005C0G1H050CT
1005	C0G	50	6	C1005C0G1H060DT
1005	C0G	50	6.8	C1005C0G1H6R8DT
1005	C0G	50	7	C1005C0G1H070DT
1005	C0G	50	8	C1005C0G1H080DT
1005	C0G	50	9	C1005C0G1H090DT
1005	C0G	50	10	C1005C0G1H100DT
1005	C0G	50	12	C1005C0G1H120JT
1005	C0G	50	15	C1005C0G1H150JT
1005	C0G	50	18	C1005C0G1H180JT
1005	C0G	50	22	C1005C0G1H220JT
1005	C0G	50	27	C1005C0G1H270JT
1005	C0G	50	33	C1005C0G1H330JT
1005	C0G	50	39	C1005C0G1H390JT
1005	C0G	50	47	C1005C0G1H470JT
1005	C0G	50	56	C1005C0G1H560JT
1005	C0G	50	68	C1005C0G1H680JT
1005	C0G	50	82	C1005C0G1H820JT
1005	C0G	50	100	C1005C0G1H101JT
1005	C0G	50	120	C1005C0G1H121JT
1005	C0G	50	150	C1005C0G1H151JT
1005	C0G	50	180	C1005C0G1H181JT
1005	C0G	50	220	C1005C0G1H221JT
1005	C0G	50	270	C1005C0G1H271JT
1005	C0G	50	330	C1005C0G1H331JT
1005	C0G	50	390	C1005C0G1H391JT
1005	C0G	50	470	C1005C0G1H471JT
1608	C0G	50	1	C1608C0G1H010CT
1608	C0G	50	1.5	C1608C0G1H1R5CT
1608	C0G	50	2	C1608C0G1H020CT
1608	C0G	50	2.2	C1608C0G1H2R2CT
1608	C0G	50	3	C1608C0G1H030CT
1608	C0G	50	3.3	C1608C0G1H3R3CT
1608	C0G	50	4	C1608C0G1H040CT
1608	C0G	50	4.7	C1608C0G1H4R7CT
1608	C0G	50	5	C1608C0G1H050CT
1608	C0G	50	6	C1608C0G1H060DT
1608	C0G	50	6.8	C1608C0G1H6R8DT
1608	C0G	50	7	C1608C0G1H070DT
1608	C0G	50	8	C1608C0G1H080DT
1608	C0G	50	9	C1608C0G1H090DT
1608	C0G	50	10	C1608C0G1H100DT
1608	C0G	50	12	C1608C0G1H120JT
1608	C0G	50	15	C1608C0G1H150JT
1608	C0G	50	18	C1608C0G1H180JT
1608	C0G	50	22	C1608C0G1H220JT
1608	C0G	50	27	C1608C0G1H270JT
1608	C0G	50	33	C1608C0G1H330JT
1608	C0G	50	39	C1608C0G1H390JT
1608	C0G	50	47	C1608C0G1H470JT
1608	C0G	50	56	C1608C0G1H560JT
1608	C0G	50	68	C1608C0G1H680JT
1608	C0G	50	82	C1608C0G1H820JT
1608	C0G	50	100	C1608C0G1H101JT
1608	C0G	50	120	C1608C0G1H121JT
1608	C0G	50	150	C1608C0G1H151JT
1608	C0G	50	180	C1608C0G1H181JT
1608	C0G	50	220	C1608C0G1H221JT
1608	C0G	50	270	C1608C0G1H271JT
1608	C0G	50	330	C1608C0G1H331JT
1608	C0G	50	390	C1608C0G1H391JT
1608	C0G	50	470	C1608C0G1H471JT
1608	C0G	50	560	C1608C0G1H561JT
1608	C0G	50	680	C1608C0G1H681JT
1608	C0G	50	820	C1608C0G1H821JT
1608	C0G	50	1000	C1608C0G1H102JT
1608	C0G	50	1200	C1608C0G1H122JT
1608	C0G	50	1500	C1608C0G1H152JT
1608	C0G	50	1800	C1608C0G1H182JT
1608	C0G	50	2200	C1608C0G1H222JT
1608	C0G	50	2700	C1608C0G1H272JT
1608	C0G	50	3300	C1608C0G1H332JT
1608	C0G	50	3900	C1608C0G1H392JT

Case Size	TC	Voltage	Cap (pF)	TDK Item Number
2012	C0G	50	3300	C2012C0G1H332JT
2012	C0G	50	3900	C2012C0G1H392JT
2012	C0G	50	4700	C2012C0G1H472JT
2012	C0G	50	5600	C2012C0G1H562JT
2012	C0G	50	6800	C2012C0G1H682JT
2012	C0G	50	8200	C2012C0G1H822JT
2012	C0G	50	10000	C2012C0G1H103JT
3216	C0G	50	4700	C3216C0G1H472JT
3216	C0G	50	5600	C3216C0G1H562JT
3216	C0G	50	6800	C3216C0G1H682JT
3216	C0G	50	8200	C3216C0G1H822JT
3216	C0G	50	10000	C3216C0G1H103JT
3216	C0G	50	12000	C3216C0G1H123JT
3216	C0G	50	15000	C3216C0G1H153JT
3216	C0G	50	18000	C3216C0G1H183JT
3216	C0G	50	22000	C3216C0G1H223JT
3216	C0G	50	27000	C3216C0G1H273JT
3216	C0G	50	33000	C3216C0G1H333JT

Case Size	TC	Voltage	Cap (pF)	TDK Item Number
1005	X7R	25	10000	C1005X7R1E103KT
1005	X7R	25	22000	C1005X7R1E223KT
1005	X7R	25	47000	C1005X7R1E473KT
1005	X7R	16	47000	C1005X7R1C473KT
1005	X5R	16	100000	C1005X5R1C104KT
1005	X5R	10	100000	C1005X5R1A104KT
1005	X5R	6.3	220000	C1005X5R0J224KT
1005	X5R	6.3	470000	C1005X5R0J474KT
1005	X5R	6.3	1000000	C1005X5R0J105KT
1005	X5R	10	100000	C1005X5R1A104KT
1608	X7R	50	10000	C1608X7R1H103KT
1608	X7R	50	22000	C1608X7R1H223KT
1608	X7R	50	47000	C1608X7R1H473KT
1608	X7R	50	100000	C1608X7R1H104KT
1608	X7R	25	100000	C1608X7R1E104KT
1608	X7R	25	220000	C1608X7R1E224KT
1608	X7R	16	220000	C1608X7R1C224KT
1608	X5R	16	470000	C1608X5R1C474KT
1608	X5R	16	1000000	C1608X5R1C105KT
1608	X5R	10	470000	C1608X5R1A474KT
1608	X5R	10	1000000	C1608X5R1A105KT
1608	X5R	6.3	2200000	C1608X5R0J225KT
1608	X5R	6.3	4700000	C1608X5R0J475KT
2012	X7R	50	220000	C2012X7R1H224KT
2012	X7R	25	470000	C2012X7R1E474KT
2012	X7R	25	1000000	C2012X7R1E105KT
2012	X5R	16	1000000	C2012X5R1C105KT
2012	X5R	16	2200000	C2012X5R1C225KT
2012	X5R	10	2200000	C2012X5R1A225KT
2012	X5R	10	4700000	C2012X5R1A475KT
2012	X5R	6.3	4700000	C2012X5R0J475KT
2012	X5R	6.3	10000000	C2012X5R0J106KT
2012	X5R	6.3	22000000	C2012X5R0J226KT
3216	X7R	50	470000	C3216X7R1H474KT
3216	X7R	50	1000000	C3216X7R1H105KT
3216	X7R	25	1000000	C3216X7R1E105KT
3216	X7R	25	2200000	C3216X7R1E225KT
3216	X7R	25	4700000	C3216X7R1E475KT
3216	X5R	16	4700000	C3216X5R1C475KT
3216	X5R	16	10000000	C3216X5R1C106KT
3216	X5R	6.3	10000000	C3216X5R0J106KT
3216	X5R	6.3	22000000	C3216X5R0J226KT
3216	X5R	6.3	47000000	C3216X5R0J476KT

Case Size	TC	Voltage	Cap (pF)	TDK Item Number
1005	Y5V	16	100000	C1005Y5V1C104ZT
1005	Y5V	10	470000	C1005Y5V1A474ZT
1608	Y5V	50	100000	C1608Y5V1H104ZT
1608	Y5V	25	474444	C1608Y5V1E474ZT
1608	Y5V	16	1000000	C1608Y5V1C105ZT
1608	Y5V	10	2200000	C1608Y5V1A225ZT
2012	Y5V	50	470000	C2012Y5V1H474ZT
2012	Y5V	50	1000000	C2012Y5V1H105ZT
2012	Y5V	25	2200000	C2012Y5V1E225ZT
2012	Y5V	16	4700000	C2012Y5V1C475ZT
2012	Y5V	10	10000000	C2012Y5V1A106ZT
3216	Y5V	50	2200000	C3216Y5V1H225ZT
3216	Y5V	25	4700000	C3216Y5V1E475ZT
3216	Y5V	16	10000000	C3216Y5V1C106ZT
3216	Y5V	10	22000000	C3216Y5V1A226ZT

6.0 Packaging

Packaging shall be done to protect the capacitors against damage during transportation or storage. TDK capacitors are available in tape and reel, bulk case, or bag packaging styles. (TDK considers 13 inch tape and reel as standard packaging style.)

6.1 Tape & Reel

6.1.1 Construction and Dimension of Taping

1) Dimensions of carrier tape

Dimensions of paper tape shall be according to Table 6.1.4.A.
Dimensions of plastic tape shall be according to Table 6.1.4.B.

2) Trailer and leader of carrier tape

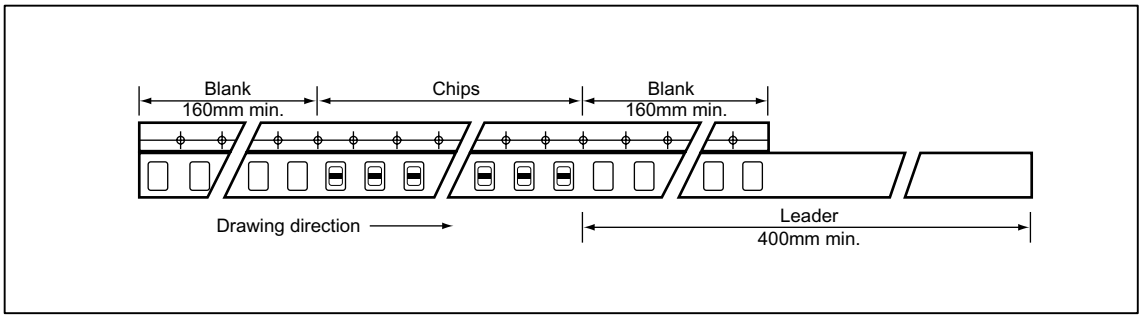


Figure 6.1.1.A: Dimensions of carrier tape

3) Dimensions of reel

Dimensions of 7 reel shall be according to Table 6.1.5.A.
Dimensions of 13 reel shall be according to Table 6.1.5.B.

4) Structure of taping

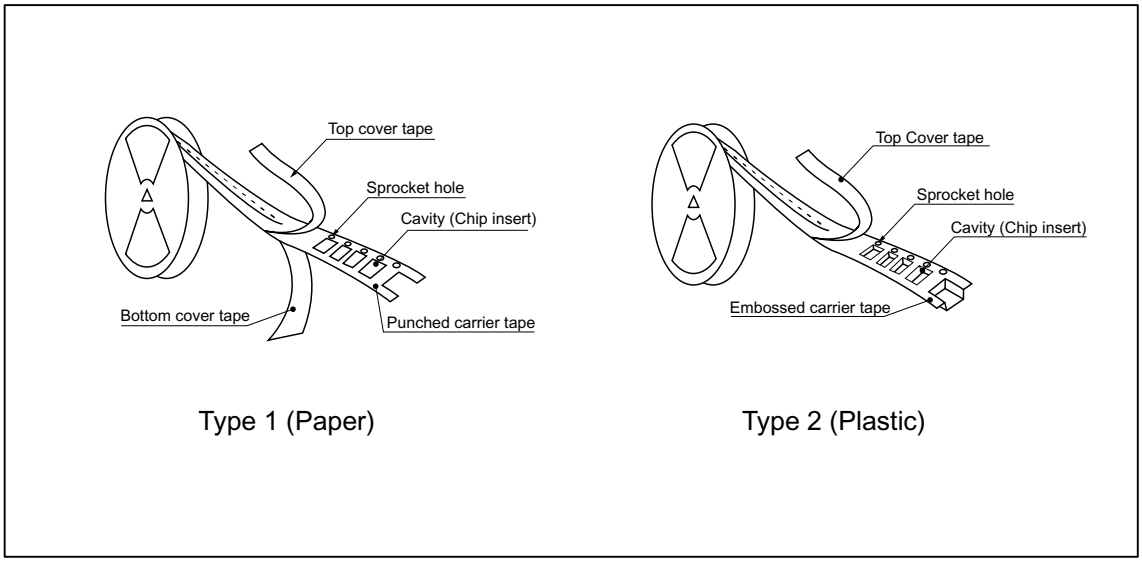


Figure 6.1.1.B: Tape Structure

6.1.2. Chip quantity

Table 6.1.2 Chip Quantity

Type	Thickness of chip	Taping material	Chip quantity	
			∅7 reel	∅13 reel
C1005	0.50 mm	Paper	10,000 pcs.	50,000 pcs.
C1608	0.80 mm	Paper	4,000 pcs.	10,000 pcs.
C2012	0.60 mm	Paper	4,000 pcs	10,000 pcs
	0.85 mm	Paper	4,000 pcs.	10,000 pcs.
	1.25 mm	Plastic	2,000 pcs.	10,000 pcs.
C3216	0.60 mm	Paper	4,000 pcs.	10,000 pcs.
	0.85 mm	Paper	4,000 pcs.	10,000 pcs
	1.15 mm	Plastic	2,000 pcs.	10,000 pcs.
	1.30 mm	Plastic	2,000 pcs.	10,000 pcs.
	1.60 mm	Plastic	2,000 pcs.	8,000 pcs.
C3225	1.25 mm	Plastic	2,000 pcs.	-----
	1.60 mm	Plastic	2,000 pcs	-----
	2.00 mm	Plastic	1,000 pcs.	-----
	2.50 mm	Plastic	1,000 pcs.	-----
C4532	2.00 mm	Plastic	1,000 pcs.	-----
	2.50 mm	Plastic	1,000 pcs.	-----
	3.20 mm	Plastic	500 pcs.	-----
C5750	2.00 mm	Plastic	500 pcs.	-----
	2.30 mm	Plastic	500 pcs.	-----
	2.50 mm	Plastic	500 pcs.	-----

6.1.3 Performance Specifications

1) Peel back strength (top tape)
   0.05 < Peel back strength < 0.7N (Figure 6.1.3.)

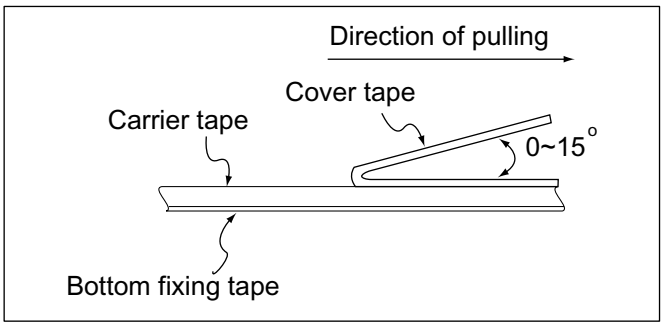


Figure 6.1.3: Peel Back Tape

2) Carrier tape shall be flexible enough to be wound around a minimum radius of 30 mm with the components in tape.
3) The number of components missing shall be less than 0.1%
4) Components shall not stick to cover tape.
5) The cover tape shall not protrude beyond the edges of the carrier tape. Cover tape shall not cover the sprocket holes.

6.1.4 Carrier tape types

6.1.4.1 Type I Paper tape

*Paper carrier tape shall be used for parts having a thickness of less than 1.0 mm

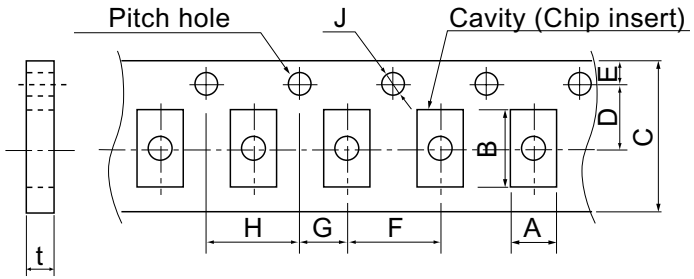


Table 6.1.4.A: Paper Carrier Tape Dimensions

(Unit : mm)

Symbol / Type	A	B	C	D	E	F	G	H	J	t
C1005	$0.65^{+0.05}_{-0.10}$	$1.15^{+0.05}_{-0.10}$	8.0 ± 0.3	3.5 ± 0.05	1.75 ± 0.1	2.0 ± 0.05	2.0 ± 0.05	4.0 ± 0.05	$\varnothing 1.5^{+0.1}_{-0.0}$	0.6 ± 0.05
C1608	1.1 ± 0.2	1.9 ± 0.2	8.0 ± 0.3	3.5 ± 0.05	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	4.0 ± 0.1	$\varnothing 1.5^{+0.1}_{-0.0}$	1.1 max.
C2012	1.5 ± 0.2	2.3 ± 0.2								
C3216	1.9 ± 0.2	3.5 ± 0.2								

6.1.4.2 Type II Plastic embossed tape

*Paper embossed tape shall be used for parts having a thickness of greater than 1.0 mm

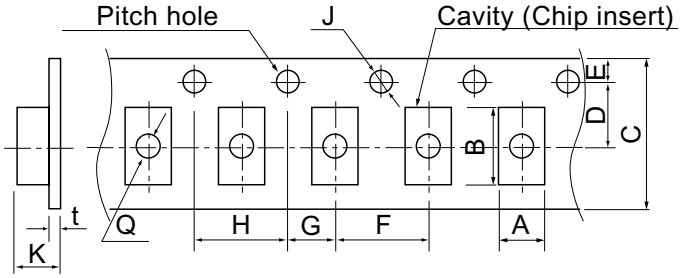


Table 6.1.4.B: Plastic Carrier Tape Dimensions

(Unit : mm)

Symbol / Type	A	B	C	D	E	F	G	H	J	K	t	Q
C2012	1.5 ± 0.2	2.3 ± 0.2	8.0 ± 0.3	3.5 ± 0.05	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	4.0 ± 0.1	∅1.5 $^{+0.1}_{-0.0}$	2.5 max.	0.3 max.	0.5 min.
C3216	1.9 ± 0.2	3.5 ± 0.2										
C3225 (2.0 mm thk)	2.9*	3.6*	8.0 ± 0.3	3.5 ± 0.05	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	4.0 ± 0.1	∅1.5 $^{+0.1}_{-0.0}$	2.5 max.	0.6 max.	0.5 min.
C3225 (2.5 mm thk)	2.9*	3.6*	12.0 ± 0.3	5.5 ± 0.05	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	4.0 ± 0.1	∅1.5 $^{+0.1}_{-0.0}$	6.5 max.	0.6 max.	0.5 min.
C4532	3.6*	4.9*	12.0 ± 0.3	5.5 ± 0.05	1.75 ± 0.1	8.0 ± 0.1	2.0 ± 0.05	4.0 ± 0.1	∅1.5 $^{+0.1}_{-0.0}$	6.5 max.	0.6 max.	1.5 min.
C5750	5.4*	6.1*										

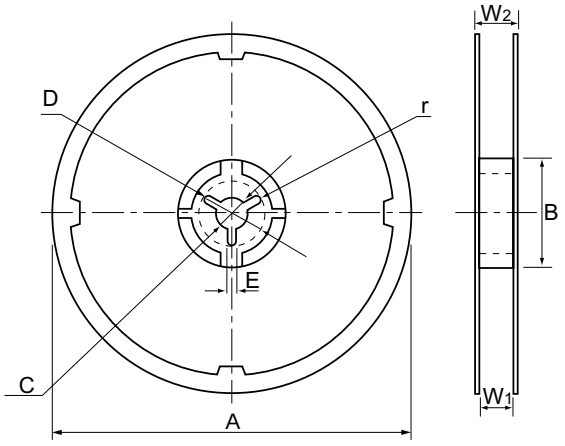
*Represents typical value and is used for reference only.

6.1.5 Reel types

Reels are available in 7 and 13 inch diameters and are made of static dissipative polystyrene.

A) 7 " Reel

REEL DIMENSIONS



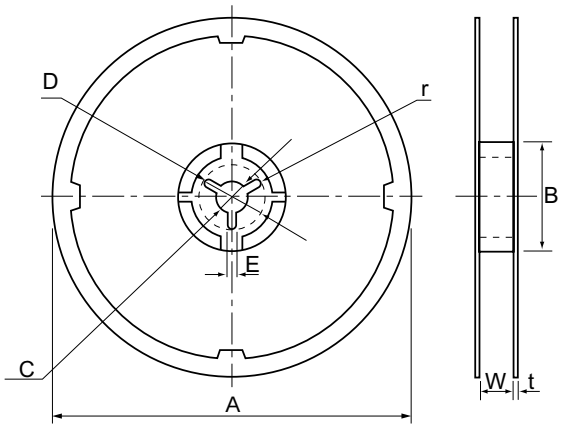
(Unit: mm)

Symbol / Case	A	B	C	D	E	W1	W2	r
C1005 (CC0402)	∅178 ± 2.0	∅60 ± 2.0	∅13 ± 0.5	∅21 ± 0.8	2.0 ± 0.5	9.0 ± 0.3	13 ± 1.4	1.0
C1608 (CC0603)								
C2012 (CC0805)								
C3216 (CC1206)								
C3225 (CC1210)								
C3225 (CC1210) 2.5 thk.	∅178 ± 2.0	∅60 ± 2.0	∅13 ± 0.5	∅21 ± 0.8	2.0 ± 0.5	13.0 ± 0.3	17.0 ± 1.4	1.0
C4532 (CC1812)								
C5750 (CC2220)								

Figure 6.1.5.A: 7 Reel Dimensions

B) 13 Reel

REEL DIMENSIONS



(Unit : mm)

Symbol	A	B	C	D	E	W	t	r
C1005 (CC0402)	∅382 max.	∅50 min.	∅13 ± 0.5	∅ 21 ± 0.8	2.0 ± 0.5	10.0 ± 1.5	2.0 ± 0.5	1.0
C1608 (CC0603)								
C2012 (CC0805)								
C3216 (CC1206)								

Figure 6.1.5.B: 13 Reel Dimensions

6.2 Bulk Case

6.2.1 Dimensions of bulk case

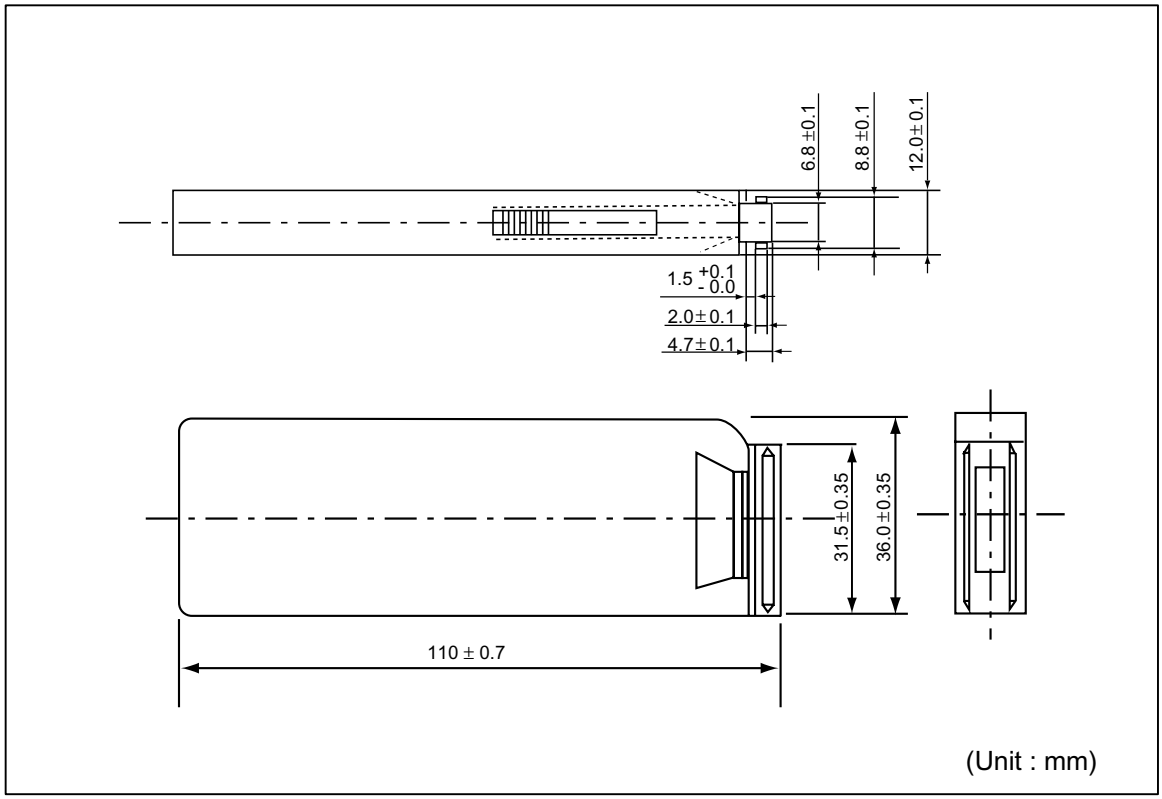


Figure 6.2.1: Dimensions of Bulk Case

6.2.2 Chip quantity

(Unit : mm)

Type	Thickness of chip	Chip quantity (pcs./ case)
C1005	0.5 ± 0.05	50,000
C1608	0.8 ± 0.07	15,000
C2012	0.6 ± 0.10	10,000
C3216	0.6 ± 0.10	5,000

Table 6.2.2: Chip Quantity

6.2.3 Accuracy of chip quantity

$^{+50}_{-0.0}$ pcs. of total quantity shall be guaranteed.

6.2.4 Material

Polycarbonate (Static dissipative)

6.3 Bulk Bag

6.3.1 Dimensions of bulk bag

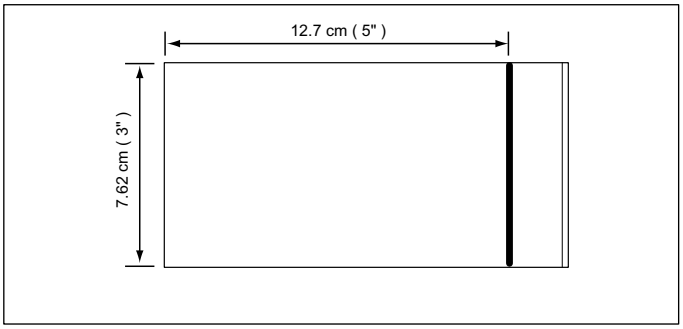


Figure 6.3.1: Bulk Bag Dimensions

6.3.2 Chip quantity

Case	Quantity/Bag
C1005	30,000
C1608	10,000
C2012	5,000
C3216	5,000

Figure 6.3.2: Quantity per Bag

6.3.3 Material

Static dissipative plastic zip lock bag.

6.4 Labeling (Applies to MLCCs manufactured at TDK Components USA, Inc. only)

The following details specifications for Reel/Bag labels.

6.4.1 Barcode Type

TDK packaging labels conform to the non-retail American Industry barcode standard "Code 39."

6.4.2 Data Identifiers

Data identifiers in human readable areas shall appear in the title area only. The identifier should be contained in parenthesis after the title itself. Identifiers included in the human readable data areas are unacceptable.

Example:

Quantity for a given package is 10,000 pcs. Human readable area should read as follows:

QTY(Q):10000

Incorrect representations would be:

QTY:Q10000
QTY(Q):Q10000

6.4.3 Data with Barcode

Human readable data corresponding to each barcode shall be between 3.0-5.0 mm. Font shall be represented in an Arial-style character.

6.4.4 Spacing

A margin (or quiet zone) of minimum dimension shall surround all barcode fields:

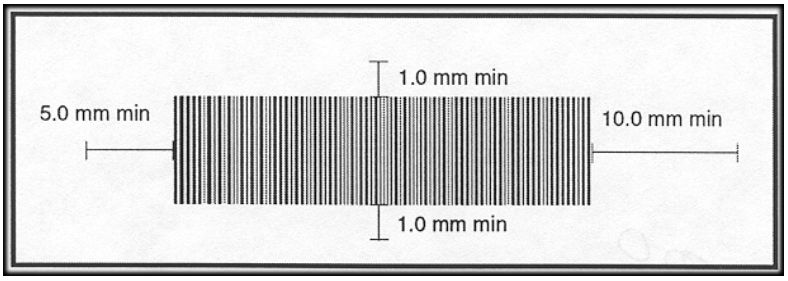


Figure 6.4.1 Barcode Field Margins

6.4.5 Other Data

Other data that is not associated with a bar-coded field shall be between 2.0-6.0 mm height, Arial Font.

6.4.6 Bisector

A 0.5 mm line shall be placed horizontally across the label 1.7 cm from label bottom edge. This line serves as a division between information most frequently used by the customer (upper area) and TDK supporting data.

6.4.6 Bar-coded Data Fields

All data fields included in the TDK Standard Label are described in this section. Examples of standard Reel/Bag and Cassette labels are shown as follows:

Figure 6.4.5A: Reel/Bag label

Figure 6.4.5B: Cassette label

1. **Customer Product ID (P)** - The customer-supplied part number in accordance with TDK customer registration.
2. **Reel #** - This field will list in ascending order the reel, bag, or cassette number as manufactured.
3. **Quantity (Q)** – Total number or pieces packaged in that reel, bag, or cassette.
4. **Vendor (V)** – Supplier ID (which will always read TDK).
5. **Lot (1T)** - The TDK Inspection Number that allows traceability of the lot.
6. **Date Code (T)** - This field contains the year and workweek the product was packaged in the format (YYWW). For example, A lot packaged on January 1, 1999 would read: 9901.
7. Fields below the **bisector** contain human readable and TDK internal processing information.

6.4.6 Human Readable Data Only

6.4.6.1 Manufacturing Site

This field contains the site of origin. For TCU standard labels, this field will read.

TDK COMPONENTS USA, INC.

6.4.6.2 TDK Item

This field contains the 18 or 19 character TDK Item for TDK reference.

6.4.6.3 Customer Name

This field contains the appropriate customer name.

6.4.6.4 Label Date

This field contains the date the label was printed in MM/DD/YY format.

7.0 Caution

Table 7.0: Caution

No.	Process	Condition
1	Storage	1) The capacitor must be stored in an ambient temperature between 5 ~ 40°C with a relative humidity of 20 ~ 70%. The products should be used within 6 months upon receipt. 2) The capacitors must be stored in an environment free of gases such as Hydrogen Sulphide, Hydrogen Sulphate, Chlorine and Ammonia. 3) Avoid storing in direct sunlight and falling of dew.
2	Circuit design ⚠Caution	2-1 Operating temperature Operating temperature should be followed strictly within this specification. 1) Do not use capacitor above the maximum allowable operating temperature. 2) Surface temperature including self heating should be below maximum operating temperature. (Due to dielectric loss, capacitor will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the surrounding area. Please design the circuit so that the maximum temperature of the capacitor including the self heating to be below the maximum allowable operating temperature.) 2-2 Operating voltage 1) Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, the peak must be below the rated voltage. With AC or pulse overshooting, the peak must be below the rated voltage. 2) Even below the rated voltage, if repetitive high frequency AC or pulse is applied, the reliability of the capacitor may be reduced. 3) Voltage derating will greatly reduce the failure rate. Since the failure rate follows the 3 power law of voltage, the failure rate used under Uw with UR rated product will be lowered as $(Uw/UR)^3$.

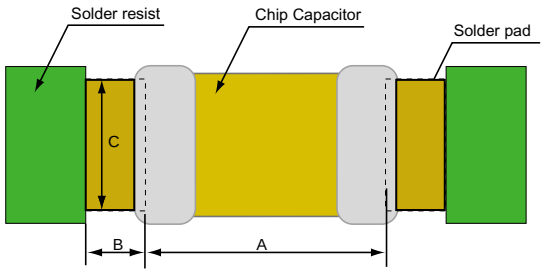
Table 7.0: Caution (continued)

<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>3</td><td>Designing P.C. board</td><td>
The amount of solder at the terminations has a direct effect on the reliability of the capacitor.

1) The greater the amount of solder, the higher the stress on the chip capacitor, and the more likely that it will break. When designing a P.C. board, determine the shape and size of the solder pads to have proper amount of solder on the terminations.

2) Avoid using common solder pads for multiple terminations and provide individual solder pads for each terminations.

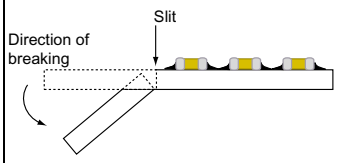
See the following table for recommended pad dimensions.

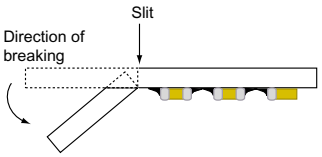


Wave (Unit : mm)
<table>
<tr><th>Type / Symbol</th><th>C1608 (CC0603)</th><th>C2012 (CC0805)</th><th>C3216 (CC1206)</th></tr>
<tr><td>A</td><td>0.7 ~ 1.0</td><td>1.0 ~ 1.3</td><td>2.1 ~ 2.5</td></tr>
<tr><td>B</td><td>0.8 ~ 1.0</td><td>1.0 ~ 1.2</td><td>1.1 ~ 1.3</td></tr>
<tr><td>C</td><td>0.6 ~ 0.8</td><td>0.8 ~ 1.1</td><td>1.0 ~ 1.3</td></tr>
</table>

Reflow Soldering (Unit : mm)
<table>
<tr><th>Type / Symbol</th><th>C1005 (CC0402)</th><th>C1608 (CC0603)</th><th>C2012 (CC0805)</th><th>C3216 (CC1206)</th><th>C3225 (CC1210)</th><th>C4532 (CC1812)</th><th>C5750 (CC2220)</th></tr>
<tr><td>A</td><td>0.3 ~ 0.5</td><td>0.6 ~ 0.8</td><td>0.9 ~ 1.2</td><td>2.0 ~ 2.4</td><td>2.0 ~ 2.4</td><td>3.1 ~ 3.7</td><td>4.1 ~ 4.8</td></tr>
<tr><td>B</td><td>0.35 ~ 0.45</td><td>0.6 ~ 0.8</td><td>0.7 ~ 0.9</td><td>1.0 ~ 1.2</td><td>1.0 ~ 1.2</td><td>1.2 ~ 1.4</td><td>1.2 ~ 1.4</td></tr>
<tr><td>C</td><td>0.4 ~ 0.6</td><td>0.6 ~ 0.8</td><td>0.9 ~ 1.2</td><td>1.1 ~ 1.6</td><td>1.9 ~ 2.5</td><td>2.4 ~ 3.2</td><td>4.0 ~ 5.0</td></tr>
</table>
</td></tr>
</table>

Table 7.0: Caution (continued)

<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>3</td><td>Designing P.C. board (Continued)</td><td>4) Recommended chip capacitor layout is as follows:
<table>
<tr><th>Subject</th><th>Disadvantage against bending stress</th><th>Advantage against bending stress</th></tr>
<tr><td>Mounting face</td><td>Perforation & slit
 

Break P.C. board with mounted side up</td><td>Perforation & slit
 

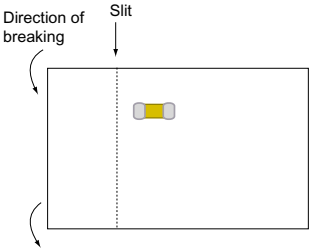
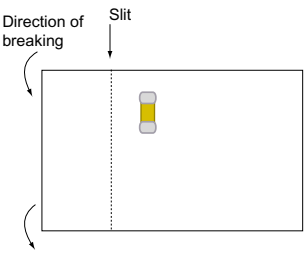
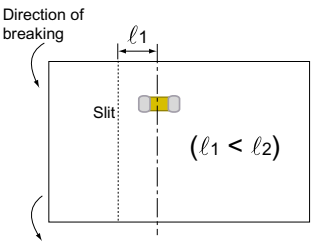
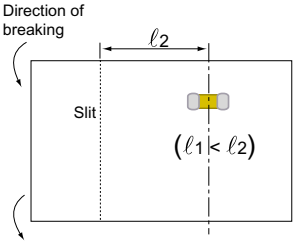
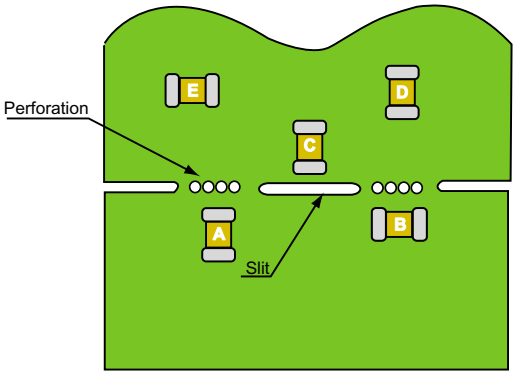
Break P.C. board with mounted side down.</td></tr>
<tr><td>Chip arrangement (Direction)</td><td>Mount perpendicular to perforation or slit
 
</td><td>Mount in parallel with perforation or slit
 
</td></tr>
<tr><td>Distance from slit</td><td>Closer to slit is higher stress
 
</td><td>Away from slit is less stress
 
</td></tr>
</table></td></tr>
</table>

Table 7.0: Caution (continued)

<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>3</td><td>Designing P.C. board
(Continued)</td><td>
5) Mechanical stress varies according to location of chip capacitors on the P.C. board.


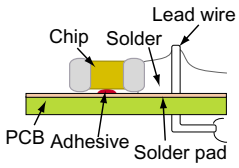
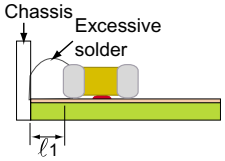
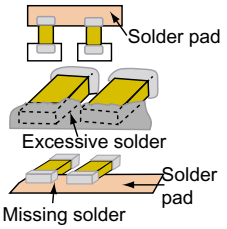
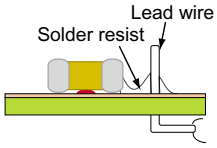
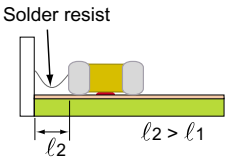
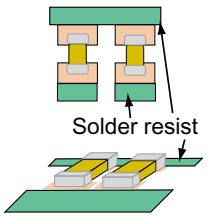
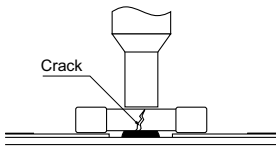
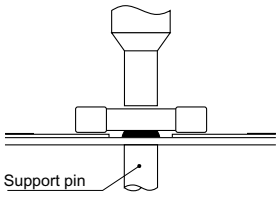
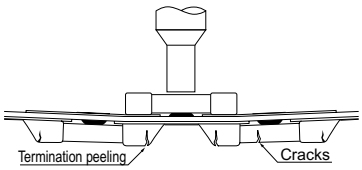
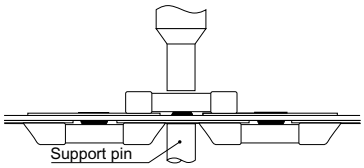
The stress in Capacitors is in the following order.
A > B = C > D > E
6) Layout recommendation
<table>
<tr><th>Example</th><th>Use of common solder land</th><th>Soldering with chassis</th><th>Use of common solder land with other SMD</th></tr>
<tr><td>Need to avoid</td><td> 
</td><td> 
</td><td> 
</td></tr>
<tr><td>Recommended</td><td> 
</td><td> 
</td><td> 
</td></tr>
</table>
</td></tr>
</table>

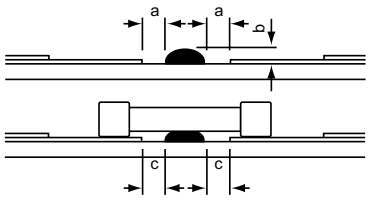
Table 7.0: Caution (continued)

<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>4</td><td>Mounting</td><td>
4-1 Stress from mounting head
If the mounting head is adjusted too low, it may induce excessive stress in the chip Capacitor resulting in cracking. Please take the following precautions.

1) Adjust the bottom dead center of the mounting head to just on the P.C. board surface and not pressing on it.
2) Adjust the mounting head pressure to be 1 to 3N of static weight.
3) To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C. board.(see following)

<table>
<tr><th>Mounting</th><th>Not recommended</th><th>Recommended</th></tr>
<tr><td>Single sided</td><td> 
</td><td> 
</td></tr>
<tr><td>Double sided</td><td> 
</td><td> 
</td></tr>
</table>
When the centering jaw is worn out, it may give mechanical impact on the capacitor to cause a crack. Please control the close up dimension of the centering jaw and provide sufficient preventive maintenance and replacement of it.

4-2 Amount of adhesive



Example : C2012 (CC0805) and C3216 (CC1206)

<table>
<tr><th>Labels</th><th>a</th><th>b</th><th>c</th></tr>
<tr><td>Dimensions</td><td>0.2mm min.</td><td>70 ~ 100 um</td><td>do not touch the solder pad</td></tr>
</table>
</td></tr>
</table>

Table 7.0: Caution (continued)

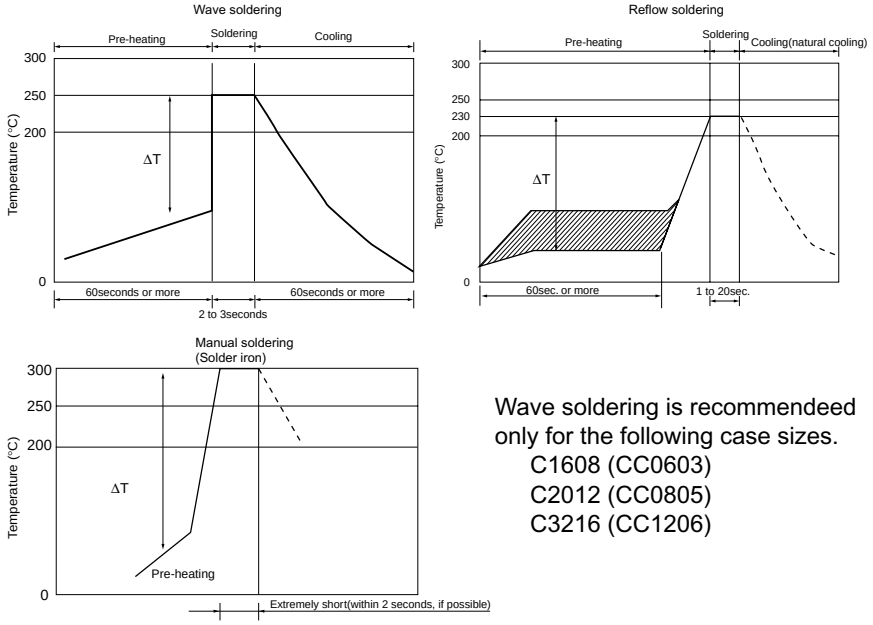
No.	Process	Condition
5	Soldering	5-1 Flux selection Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitors. To avoid such degradation, the following is recommended. 1) It is recommended to use a mildly activated rosin flux (less than 0.1 wt% chlorine). Strong flux is not recommended. 2) Excessive flux must be avoided. Please provide proper amount of flux. 3) When water-soluble flux is used, enough washing is necessary. 5-2 Recommended soldering profile by various methods  Wave soldering is recommendeed only for the following case sizes. C1608 (CC0603) C2012 (CC0805) C3216 (CC1206) 5-3 Avoiding thermal shock 1) Preheating condition **Soldering** / **Size** / **Temp. (°C)** Wave soldering / C3216 (CC1206) or less / ΔT ≤ 150 Reflow soldering / C3216 (CC1206) or less / ΔT ≤ 190 Reflow soldering / C3225 (CC1210) or more / ΔT ≤ 130 Manual soldering / C3216 (CC1206) or less / ΔT ≤ 190 Manual soldering / C3225 (CC1210) or more / ΔT ≤ 130 2) Cooling condition Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (△T) must be less than 100°C.

Table 7.0: Caution (continued)

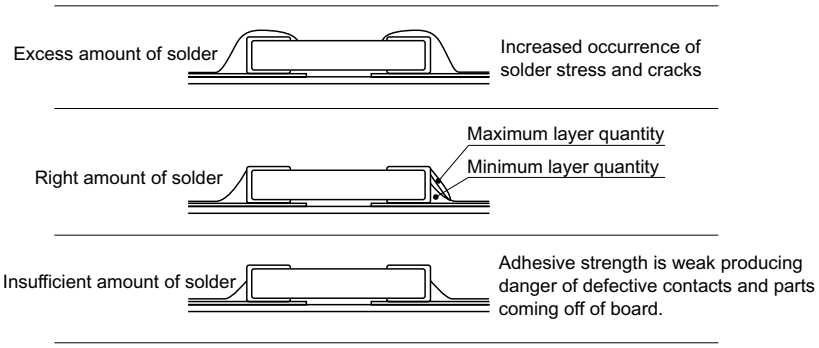
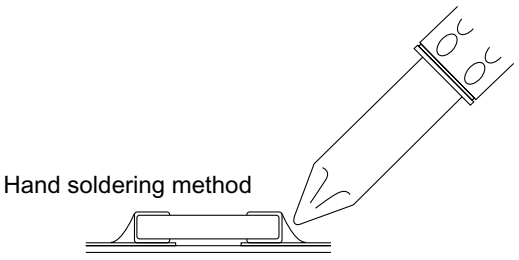
No.	Process	Condition
5	Soldering (Continued)	5-4 Amount of solder Excessive solder will induce higher tensile force in chip capacitor when temperature changes and may result in chip cracking. Insufficient solder may detach the capacitor from the P.C. board.  5-5 Solder repair by solder iron 1) Selection of the soldering iron tip Tip temperature of solder iron varies by its type, P.C. board material and solder pad size. Higher tip temperature may be faster, but the heat shock may crack the chip capacitor. (Following conditions are recommended.) **Temp. (°C)** / **Wattage (W)** / **Shape (mm)** 300 MAX. / 20 MAX. / ∅3.0 MAX. 2) Direct contact of the soldering iron with ceramic dielectric of chip capacitor may cause cracking. Do not make contact directly with the ceramic dielectric. 

Table 7.0: Caution (continued)

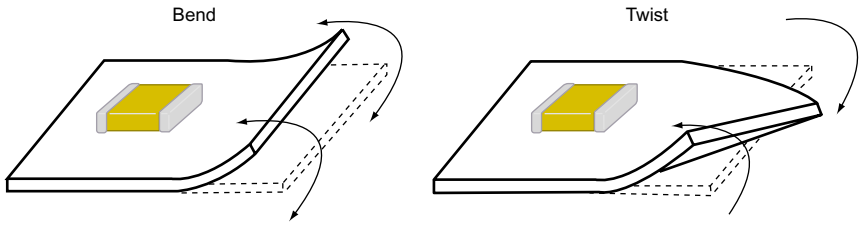
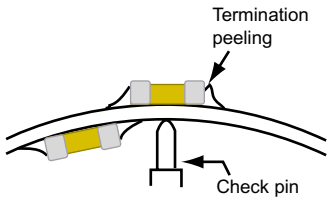
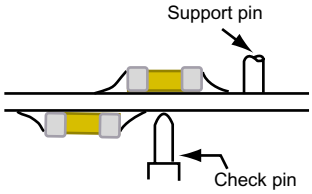
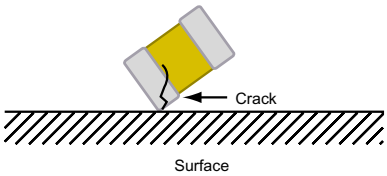
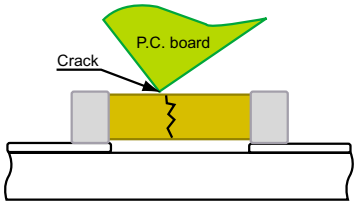
No.	Process	Condition
6	Cleaning	1) If an unsuitable cleaning fluid is used, flux residue or some foreign article may stick to chip capacitor surface causing deteriorated performance, especially insulation resistance. 2) If the cleaning condition is not suitable, it may damage the chip capacitor. 2-1) Insufficient washing (1) Lead wire and terminal electrodes may corrode due to Halogen in the flux. (2) Halogen in the flux may adhere on the surface of capacitor, and lower the insulation resistance. (3) Water soluble flux has higher tendency to have the above mentioned problems (1) and (2). 2-2) Excessive washing (1) Excessive washing may damage the coating material of coated capacitor and deteriorate it. (2) When ultrasonic cleaning is used, excessively high ultrasonic energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, use the following recommended condition. Power : 20W/l max. Frequency : 40kHz max. Washing time : 5 minutes max. 2-3) If the cleaning fluid is contaminated, the density of Halogen increases, and it may bring the same result as insufficient cleaning.
7	Coating and molding of the P.C. board	1) When the P.C. board is coated, verify the quality influence on the product. 2) Verify that there is no harmful decomposing or reaction gas emittion during curing. 3) Verify the curing temperature.
8	Handling after chip is mounted	1) Please pay attention not to bend or distort the P.C. board after soldering in handling and storage, otherwise the chip capacitor may crack or dislodge. Avoid the following: 

Table 7.0: Caution (continued)

<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>8</td><td>Handling after chip is mounted (Continued)</td><td>2) When functional check of the P.C. board is performed, check pin pressure as it tends to be adjusted higher for fear of loose contact. If the pressure is excessive and bends the P.C. board, it may crack the chip capacitor or peel the terminations off.

Adjust the check pins not to bend the P.C. board.
<table>
<tr><th>Item</th><th>Not recommended</th><th>Recommended</th></tr>
<tr><td>Board bending</td><td> 
</td><td> 
</td></tr>
</table></td></tr>
<tr><td>9</td><td>Handling of loose chip capacitor</td><td>1) If dropped the chip capacitor may crack. Once dropped do not use it. This is especially true for large case sized chips.
 

2) Avoid piling up P.C. boards after mounting. The corner of the P.C. board may hit the chip capacitor of another board causing the chip to crack or dislodge.
 
</td></tr>
<tr><td>10</td><td>Others</td><td>If a capacitor fails in medical, aerospace or nuclear equipment, it may incur extensive loss of life and damage in society. For such purposes specially designed high reliability capacitors must be used.</td></tr>
</table>

8.0 Disposal

Dispose this product as industrial waste in accordance with local Industrial Waste regulations.

End of specification